A Differentially-tuned CMOS LC VCO for Low-Voltage Full-Rate 10 Gb/s CDR Circuit

Debanjan Mukherjee, Jishnu Bhattacharjee and Joy Laskar

Yamacraw Design Center, Georgia Institute of Technology, Atlanta Georgia 30332

Email: debanjan@ece.gatech.edu

Abstract — **A fully-integrated differentially-tuned CMOS LC voltage controlled oscillator (VCO) is presented. The VCO is designed in a 0.13 μm standard digital CMOS process with a 1.2 V supply. It achieves a phase noise of -99 dBc/Hz at 1 MHz offset from a carrier frequency of 10 GHz and has a tuning range of 3.7 GHz with the core consuming only 3.6mW of dc power. This satisfies the requirements of clock-and-data-recovery (CDR) circuits for 10 gigabit optical communication systems. This paper also investigates, for the first time, the circuit topologies of other building blocks for a fully-differential implementation of a closed loop full-rate CDR circuit with low supply voltage (1.2 V).**

I. Introduction

With the exploding demands for bandwidth, fiber-optic systems, e.g. SONET OC-192 and 10-gigabit ethernet (IEEE 802.3ae) have received a great amount of interest in recent times. Optical ethernet extends the reach of ethernet beyond the local-area-networks (LANs) into metropolitan-area-networks (MANs) and wide-area-networks (WANs). However, the design of low-cost opto-electronic transceivers for these systems remains a challenge.

With scaling, CMOS technology proves to be a viable option for designing front-end circuitry for high-speed optical communication systems. The 0.13 μm digital CMOS process used in this design has a f_T of more than 65 GHz. CMOS technology offers higher level of integration and lower cost over the III-V semiconductor and silicon bipolar technologies. Low supply voltage (1.2 V in this case), however, makes design of the analog front-end very challenging.

One of the critical blocks in these receivers is the clock and data recovery unit which retrieves the clock from non-return-to-zero (NRZ) random data stream. An important component of closed loop CDR circuits is the VCO. Considering high frequency and stringent jitter requirements for current standards, LC resonator based oscillators are preferred to relaxation or ring oscillators. Also, a fully differential architecture is preferable for both control and signal paths in order to reduce sensitivity to any common mode perturbations e.g., supply and substrate noise. This paper presents the design of a differentially-tuned CMOS LC VCO. The VCO meets the requirements of SONET OC-192 systems. The differential tuning essentially implies making the charge pump differential which necessitates common mode feedback. The circuit topologies of other building blocks for a fully-differential implementation of a CDR circuit based on charge-pump phase-locked-loop techniques are also presented.

Organization of the paper is as follows: VCO phase noise requirements and design issues are discussed in section II, inductor design is described in section III, design of the differentially tuned varactor is presented in section IV, circuit topologies for other CDR building blocks are addressed in section V, section VI discusses results and section VII concludes the paper.

II. VCO Phase Noise Requirements And Design Issues

The GR-253-CORE for SONET OC-192 systems specifies rms jitter generation to be less than 0.01 U.I. (unit interval). In a closed loop system, the VCO timing jitter increases with square root of time but it reaches a saturation level for time greater than the loop time constant [1]. The feedback loop tracks the timing uncertainties which are slower than the loop bandwidth. For an rms timing jitter of 1 ps (0.01 U.I), the open-loop VCO phase noise requirement is calculated to be -90 dBc/Hz @ 1 MHz offset from the carrier frequency of 10 GHz, considering a loop bandwidth of 10 MHz.

A differential LC VCO topology with an nMOS cross-coupled core and a pMOS tail current source (Fig. 1) is suitable for low voltage operation satisfying the phase noise requirement. Though a pMOS core has better phase noise performance [2], an nMOS core is chosen as the latter has a better tuning range. A pMOS tail current source is preferred to its nMOS counterpart because: (a) the pMOS current source taps the tank-common mode point which has less variation from an ac perspective compared to the common-source point tapped by the nMOS source, (b) pMOS has less flicker noise. Differential tuning is obtained as in the bipolar VCO of [3] by cascading the varactors with fixed capacitors and applying a differential control voltage as shown in Fig. 1. The tail current value is

0-7803-7239-5/02/$10.00 © 2002 IEEE

chosen to be 3 mA such that the VCO operates in the transition period from *current-limited* to *voltage-limited* region. The area of the tail current source is kept large keeping W/L small, such that flicker noise is reduced without increasing thermal noise. Transconductances of the active devices are kept small to have lower thermal noise but sufficiently large to meet the start-up constraint.

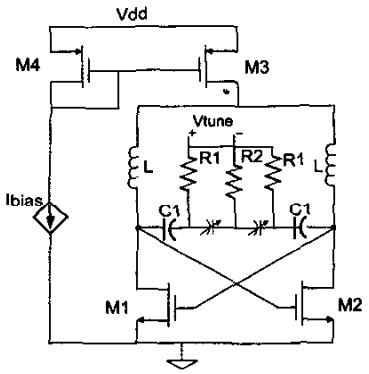

Fig. 1. Differentially-tuned LC VCO

N-MOS differential buffers have been used with inductive peaking to minimize the higher harmonic content of the output waveforms from single-ended perspective.

III. Inductor Design

The choice of inductance value plays a critical role in phase noise performance of an LC VCO. For better phase noise performance, a smaller inductance value is preferred [4] so long as it satisfies the start-up constraint. Based on this observation, an inductance value of 1.5nH (0.75 nHx2) is chosen for our design. An optimal planar spiral structure for a targeted inductance of 0.75 nH is obtained using ASITIC simulation tool [5]. Being an 8-metal-layer process, the 0.13 μm CMOS offers possibilities of realizing inductors with quality factors (Q) higher than those typically obtained in a 5-metal-layer CMOS process because it enables stacking of metal layers to reduce the series resistance without significant lowering of the self-resonant frequency. Table I lists the simulated results of expected quality factors (at 10 GHz) and self-resonant frequencies for a square inductor of length 135 μm, trace-width 10 μm, spacing 2.5 μm and 1.75 turns, as metal layers are stacked. It is seen that diminishing returns are obtained with more stacking. With this consideration, stacking of the upper 4 metal layers is used for the chosen inductor structure. Fig. 2 shows the net differential Q of the inductor-pair across the tank. Since the one-port quality factor is higher looking from the outer terminal, outer ends are connected to the oscillation nodes.

TABLE I
Q AND SELF-RESONANT FREQUENCY WITH STACKING OF DIFFERENT METAL LAYERS

No. of stacked layers	Single ended Q	Self-resonant freq (GHz)
1 (m8)	9	45
2 (m8/7)	11	44
3 (m8/7/6)	11.5	41
4 (m8/7/6/5)	12	37.5
5(m8/7/6/5/4)	12	35

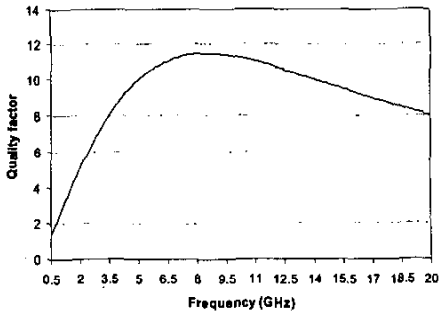

Fig. 2. Differential Q of the inductor pair across the tank

IV. Varactor Design

We have used MOS accumulation varactor with n+ contacts in n-well which offers monotonic capacitance-vs.-voltage profile and does not require any additional mask. The accumulation mode varactor has higher capacitance per unit area and higher quality factor and tuning range compared to reverse-biased pn junction and MOS depletion/inversion varactors. The basic trade-off is between tuning range and quality factor. Shorter gate-length improves quality factor by reducing n-well series resistance but decreases the tuning range by increasing the ratio of fixed overlap capacitance to the variable capacitance. The varactor has a quality factor of more than 20 with a tuning ratio ($C_{v,max}/C_{v,min}$) close to 5.5. Fig. 3 shows the capacitance profile of the designed varactor with the voltage applied across the gate and source/drain terminals. Any p or n-type low-drain-diffusion is avoided. The variable capacitance can be approximately modeled as hyperbolic-tangent or higher order polynomial function of gate to source/drain voltage. The common mode voltage of the oscillation nodes is chosen such that maximum tuning is obtained when varactor control voltage is varied from 0 to V_{dd}.

To obtain differential tuning, varactors are connected as shown in Fig. 1. The equal valued fixed capacitors (C_1) used in the configuration have two purposes: (a) couple the

oscillation signal with the varactors, (b) block the dc-tuning voltage applied across the varactors from appearing on the oscillation nodes. A value of 800 fF has been chosen for the fixed capacitors such that, in conjunction with the varactors and the parasitic circuit capacitance, an acceptable frequency tuning range is obtained. Resistance R_1 has been kept much larger (20 Kohm) compared to the ac impedance offered by the fixed capacitors around 10 GHz. R_2 has been kept at 10 Kohm, half the value of R_1, so that both gate and the source/drain terminals of the varactors see same resistance from common-mode perspective. Gate terminals are connected to the oscillation nodes (via fixed capacitors) so that n-well to substrate capacitance appears as common-mode and does not load the tank.

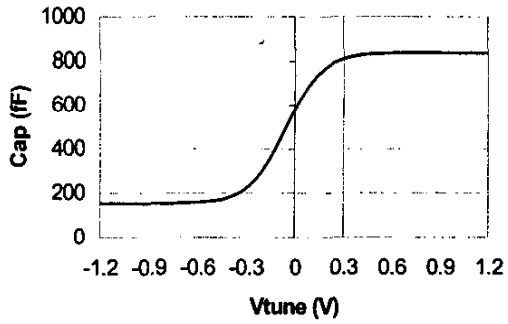

Fig. 3. Varactor capacitance vs. voltage profile

V. Other Building Blocks For CDR

In this section circuit topologies, operable at 1.2 V supply, for other building blocks of a fully differential full-rate CDR circuit based on charge-pump PLL techniques are presented.

A. Phase Frequency Detector

Any clock recovery scheme essentially means generation of a periodic output which is locked to the input data but has inertia to resist any drift in the event of missing data transitions. This necessitates the implementation of a phase frequency detector (PFD) which is less sensitive to missing pulses in the random input data. A topology that achieves reduced sensitivity to data transition density is the modified triwave phase detector [6]. The challenge in realizing this topology, as technology scales, is the low supply voltage, which makes stacking of the transistors difficult. The conventional source coupled latches suffer from this problem. A latch topology that can operate at low supply voltage is shown in Fig. 4 [7].

Symmetric XOR gate topology shown in Fig. 5 reduces systematic phase offset [8]. Resistive loading is used at the current summing junction of transistors M3 and M4 to avoid transistor stacking.

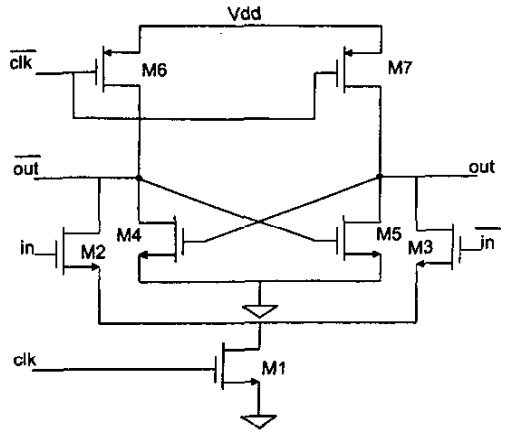

Fig. 4. Low-voltage latch for PFD

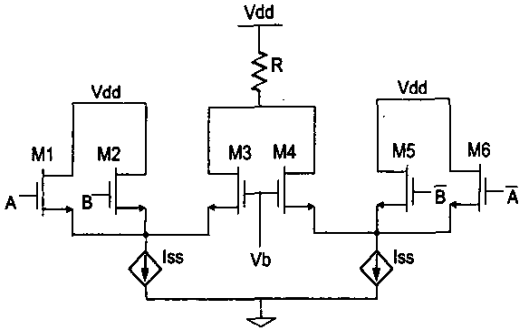

Fig. 5. Symmetric XOR gate

The summation of the four XOR outputs of the modified triwave PFD has been achieved implicitly in the differential charge-pump topology discussed in the next section.

B. Charge pump and the loop filter

The differential charge-pump topology is shown in Fig. 6. It is similar to that in reference [9]. The only difference is the inclusion of two extra pMOS devices to implement the summation of four XOR outputs in the PFD.

The loop filter must be designed to provide required filtering while maintaining the loop stability. A second order loop filter is chosen for this design. The additional pole provides more suppression of spurious signals and control line ripples but the extra phase lag sacrifices stability. The resistor and capacitor values have been chosen such that for a given loop bandwidth (10 MHz for this case) the design maximizes phase margin.

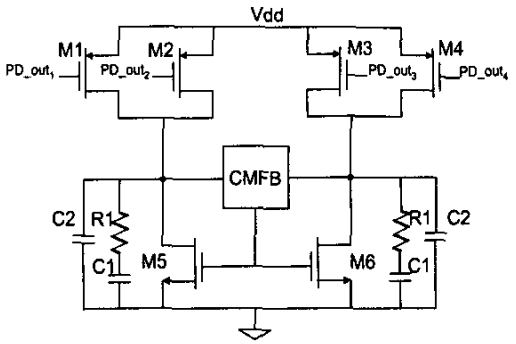

Fig. 6. Differential charge pump and loop filter

VI. Results

Fig. 7 shows the phase noise spectrum of the VCO for a center frequency of 10 GHz. Phase noise @1 MHz offset from the carrier is –99 dBc/Hz that meets the SONET OC-192 requirements with 9 dB margin. 3.7 GHz tuning range is obtained for differential control voltage variation from –0.6V to 0.6V. Phase noise variation at a particular frequency offset is within 2.5 dB throughout the tuning range. The VCO core draws 3mA of dc current from a 1.2 V supply. The VCO layout is shown in Fig. 8.

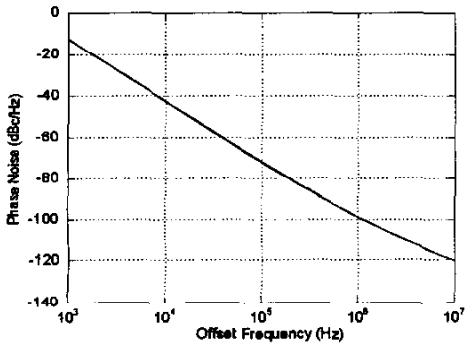

Fig. 7. VCO phase noise at 10 GHz

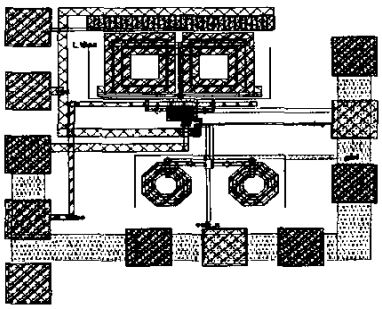

Fig. 8. Layout of the VCO

VII. Conclusion

A fully integrated differentially tuned 10 GHz LC VCO has been designed in a 0.13 μm standard digital CMOS process with 1.2 V supply. The VCO has a phase noise performance of –99 dBc/Hz at 1MHz offset that meets the phase noise requirement of a CDR circuit for the SONET OC-192 standard with 9 dB margin. Its tuning range of 3.7 GHz is sufficient to account for process, voltage, and temperature variations as well as to incorporate bit-rate enhancement due to forward error correction coding currently being implemented in optical communication systems. We have also investigated, for the first time, circuit topologies for the other building blocks of a fully differential full-rate charge-pump PLL-based CDR circuit operable with a low supply voltage of 1.2 V.

Acknowledgement

The authors wish to acknowledge the support National Semiconductor and express special thanks to Abhijit Phanse for helpful technical discussions.

References

[1] J. A. McNeill, "Jitter in Ring Oscillators," *IEEE JSSC,* vol. 32, no. 6, pp. 870-879, June 1997.

[2] C- M. Hung, et al, "Fully integrated 5.35-GHz CMOS VCOs and Prescalars," *1999 IEEE Trans on MTT*, vol. 49, no.1, pp. 17-22, Jan 2001.

[3] H. Cong, et al, "A 10Gb/s 16:1 multiplexer and 10GHz Clock Synthesizer in 0.25μm SiGe BiCMOS," *2001 ISSCC. Dig.*, pp. 80-81, Feb 2001.

[4] D. Ham and A. Hajimiri, "Concepts and Methods of Optimization of integrated LC VCOs," *IEEE JSSC.*, vol. 36, no. 6, pp. 896-909, June 2001.

[5] ASITIC: http://formosa.eecs.berkeley.edu/~niknejad/asitic.html.

[6] T. H. Lee, J. F. Bulzacchelli, "A 155-MHz clock recovery delay-and phase-locked loop," *IEEE JSSC.*, vol. SC-27, pp. 1736-1746, Dec 1992.

[7] HongMo Wang, "A 1.8V 3mw 16.8GHz frequency divider in 0.25μm CMOS," *2000 ISSCC. Dig.*, pp. 196-197, Feb 2000.

[8] B.Razavi, et al, "Design Techniques for low-voltage high-speed digital bipolar circuits," *IEEE JSSC.*, vol. 29, no.3, pp. 332-339, March 1994.

[9] J. Savoj and B.Razavi, "A 10-Gb/s CMOS clock and recovery circuit with a half-rate linear phase-detector," *IEEE JSSC.*, vol. 36, no.5, pp. 761-767, May 2001.